Pf-2944/nec/us/mh

What is claimed is :

1. A stacked capacitor comprises :

a dielectric layer ;

a two-dimensional array of terminal electrodes on at least one of first and second surfaces of said dielectric layer ;

first internal electrodes stacked in multi-levels in said dielectric layer, and said first internal electrodes being electrically connected to a power line ;

second internal electrodes stacked in multi-levels in said dielectric layer, and said second internal electrodes being electrically connected to a ground line ;

vias in said dielectric layer, so that said terminal electrodes being electrically connected through said vias to said first and second internal electrodes.

2. The stacked capacitor as claimed in claim 1, wherein said two-dimensional array of terminal electrodes are provided on both said first and second surfaces of said dielectric layer.

3. The stacked capacitor as claimed in claim 1, wherein said two-dimensional array of terminal electrodes comprises alternating alignments of said terminal electrodes connected to said power line and said terminal electrodes connected to said ground line.

4. The stacked capacitor as claimed in claim 1, wherein said via connected through said terminal electrode to said power line is electrically isolated from said first and second internal electrodes.

5. The stacked capacitor as claimed in claim 1, further comprising a low dielectric layer around said via, and said via is separated from said dielectric layer by said low dielectric layer, and said low dielectric layer has a lower dielectric constant than said dielectric layer.

6. The stacked capacitor as claimed in claim 5, wherein said dielectric constant of said low dielectric layer is at least 40.

7. The stacked capacitor as claimed in claim 5, wherein said via comprises a metal containing a glass material.

8. The stacked capacitor as claimed in claim 5, wherein said via comprises a metal containing a metal oxide material.

9. The stacked capacitor as claimed in claim 1, wherein said dielectric layer comprises a perovskite-structured compound.

10. A semiconductor device comprising :

a printed circuit board ;

a semiconductor integrated circuit ; and

a stacked capacitor which further comprises :

a dielectric layer ;

a two-dimensional array of terminal electrodes on at least one of first and second surfaces of said dielectric layer ;

first internal electrodes stacked in multi-levels in said dielectric layer, and said first internal electrodes being electrically connected to a power line ;

second internal electrodes stacked in multi-levels in said dielectric layer, and said second internal electrodes being electrically connected to a ground line ; and

vias in said dielectric layer, so that said terminal electrodes being electrically connected through said vias to said first and second internal electrodes.

11. The semiconductor device as claimed in claim 10, wherein said stacked capacitor is interposed between said printed circuit board and said semiconductor integrated circuit.

12. The semiconductor device as claimed in claim 10, wherein said stacked capacitor is provided on a first surface of said printed circuit board and a second surface of said printed circuit board.

13. The semiconductor device as claimed in claim 10, wherein said

two-dimensional array of terminal electrodes are provided on both said first and second surfaces of said dielectric layer.

14. The semiconductor device as claimed in claim 10, wherein said two-dimensional array of terminal electrodes comprises alternating alignments of said terminal electrodes connected to said power line and said terminal electrodes connected to said ground line.

15. The semiconductor device as claimed in claim 10, wherein said via connected through said terminal electrode to said power line is electrically isolated from said first and second internal electrodes.

16. The semiconductor device as claimed in claim 10, further comprising a low dielectric layer around said via, and said via is separated from said dielectric layer by said low dielectric layer, and said low dielectric layer has a lower dielectric constant than said dielectric layer.

17. The semiconductor device as claimed in claim 16, wherein said dielectric constant of said low dielectric layer is at least 40.

18. The semiconductor device as claimed in claim 16, wherein said via comprises a metal containing a glass material.

19. The semiconductor device as claimed in claim 16, wherein said

via comprises a metal containing a metal oxide material.

20. The semiconductor device as claimed in claim 10, wherein said dielectric layer comprises a perovskite-structured compound.